SIERRA SEMICONDUCTOR

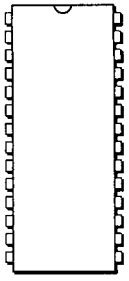
T-52-33-43

SC15025/SC15026
HiCOLOR-24™ Palette with 16.8 Million Colors

FEATURES

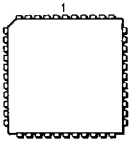
- ☐ Supports 16.8 million colors (HiCOLOR-24™)
- ☐ Supports 65,536 colors (HiCOLOR-16™)
- ☐ Supports 32,768 colors (HiCOLOR-15™)
- ☐ Supports 256 colors (pseudo color format)
- ☐ On-chip voltage reference
- ☐ Three 256 x 8 color LUT RAMs for all color modes
- ☐ Triple 6-bit or 8-bit DACs
- ☐ Analog Output Comparators
- ☐ Standard Microprocessor Interface
- ☐ Gamma correction
- ☐ 15 x 24 Overlay Registers (SC15026)
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Anti-Sparkle Circuitry
- ☐ Sync on all Three Channels (SC15026)
- ☐ Programmable Pedestal (SC15026)
- ☐ +5V CMOS
- ☐ Available Clock Rates for Pseudo Color
  - • 125 MHz • 80 MHz
  - • 110 MHz • 66 MHz
- ☐ Power-on-reset

28-PIN DIP PACKAGE



SC15025CN

44-PIN PLCC PACKAGE



SC15025CV
SC15026CV

GENERAL DESCRIPTION

The SC15025/SC15026 is a family of 24-bit VGA compatible True Color palettes with the capability to display up to 16.8 million colors simultaneously in both RGB and BGR formats. The SC15025/SC15026 also supports both the HiCOLOR-15™ format which uses 5 bits of data per primary color and the HiCOLOR-16™ format which uses 5 bits for the red, 6 bits for the green, and 5 bits for the blue primary color. The total colors available simultaneously using the HiCOLOR-15™ format are 32,768 while the HiCOLOR-16™ format

BLOCK DIAGRAM

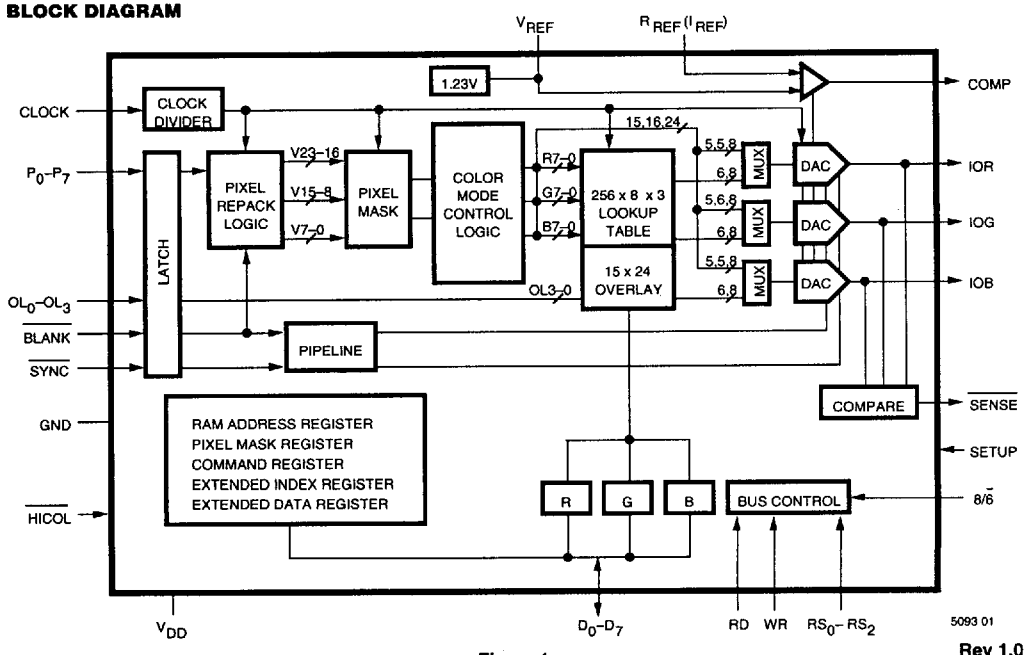


Figure 1.

Rev 1.0

provides 65,536 colors. The SC15025/SC15026 also supports 8 bit pseudo color (256 colors) mode.

Also supported is anti-aliasing and gamma correction capability—techniques which can significantly improve the graphics quality by smoothing jagged edges. This technique requires a large number of different colors and can be easily implemented with the large number of colors and three 256 x 8 color Lookup Table (LUT) RAMs offered by the SC15025/SC15026 family.

The SC15025/SC15026 features a standard 8-bit wide input pixel data port. The input pixel data is converted into either a 16-bit or 24-bit internal pixel data by the pixel repack logic. The palette family can be configured to display two windows, with 32,768 simultaneous colors from a palette of 16.8 million colors in each window. The SC15025/SC15026 is pin, function and register compatible with all the Sierra SC1148X HiCOLOR™ palette families.

The SC15026 offers three 8-bit D/A converters, three 256 x 8 color lookup tables, and 15 overlay registers. It may be configured for either 6 bits or 8 bits per color operation in the 256 color mode.

In pseudo color mode the SC15026 includes 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels and a programmable pedestal (0 or 7.5 IRE) are supported in the SC15026. Use of either an external or internal voltage reference is supported in SC15025CV/SC15026CV. An external current reference is supported in the SC15026CN.

The SC15025 is similar to the SC15026, but has no overlays or sync information on the analog outputs.

On-chip analog comparators are included to simplify diagnostics and debugging using the output of the $\overline{\text{SENSE}}$ pin. Also included is an on-chip voltage reference to simplify using the device.

The palettes operate in Pseudo Color mode when the HiCOLOR™ and true color modes are not activated.

The true color palette generates RS-343A compatible red, green, and blue video signals, capable of driving a doubly-terminated 75Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75Ω load, without external buffering.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER			DESCRIPTION
	SC15026	SC15025		
	PLCC	PLCC	DIP	
$8/\overline{6}$	2*			**8-BIT/$\overline{6}$-BIT SELECT INPUT (TTL COMPATIBLE).** This bit, in conjunction with Bit 0 of the Auxiliary Control register, specifies whether the microprocessor is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D_7 is the most significant data bit during color read/write cycles. For 6-bit operation, D_5 is the most significant bit during color read/write cycles (D_6 and D_7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC15026.
$\overline{\text{BLANK}}$	7	7	16	**COMPOSITE BLANK CONTROL INPUT (TTL COMPATIBLE).** A logic zero drives the analog outputs to the blanking level, as illustrated in Fig. 3 and 4 . It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
CLOCK	40	40	13	**CLOCK INPUT (TTL COMPATIBLE).** The rising edge of CLOCK latches the P_0–P_7, OL_0–OL_3, SYNC, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
COMP	29	29		**COMPENSATION PIN.** A 0.1 µF ceramic capacitor must always be used to bypass this pin to V_{AA}. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.
D_0–D_7	8–15	8–15	17–24	**DATA BUS (TTL COMPATIBLE).** Data is transferred into and out of the device over this eight bit bidirectional data bus. D_0 is the least significant bit.
GND	3, 24	3, 24	14	**GROUND.** All GND pins must be connected.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER SC15026 PLCC	PIN NUMBER SC15025 PLCC	PIN NUMBER SC15025 DIP	DESCRIPTION
$\overline{HICOL}$	20	20		**HICOLOR™ MODE SELECT INPUT (TTL COMPATIBLE).** This signal is inverted and logical ORed with D_7 of the command register for compatibility with the SC1148X HiCOLOR™ family. A logic zero will enable either Repack mode 1a or Repack mode 1b) selected by the D_5 bit of the command register. See Table 2 for details. The $\overline{HICOL}$ pin should be tied to V_{AA} to disable hardware selection of the HiCOLOR™ mode.
IOR, IOG, IOB	25–27	25–27	1–3	**RED, GREEN, AND BLUE CURRENT OUTPUTS.** These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable.
R_{REF}	28	28		**FULL SCALE ADJUST CONTROL.** Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full scale output current. When using an external or internal voltage reference (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: RSET (Ω) = K • 1000 • V_{REF} (V)/I_{OUT} (mA) K is defined in the table below for doubly-terminated 75 Ω loads.
I_{REF}	—	—	4	When using an external current reference (Figures 7) the relationship between I_{REF} and the full scale output current on each output is: I_{REF} (mA) = I_{OUT} (mA)/K K is defined in the table below for doubly-terminated 75 Ω loads.

Part Number	Mode	Pedestal	K
SC15025CV	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
SC15026CV	8-bit	0.0 IRE	3.025
SC15025CN	8-bit	0.0 IRE	2.236

N/C	30	2, 5, 19, 23, 30, 41–44		Not Connected. Pins 2, 5, 19, 23, 41–44 are recommended to be tied to GROUND.
OL_0–OL_3	41–44			**OVERLAY SELECT INPUTS (TTL COMPATIBLE).** These inputs specify which palette is to be used to provide color information, as illustrated in Table 7. When accessing the overlay register, the P_0–P_7 inputs are ignored. They are latched on the rising edge of CLOCK. OL_0 is the LSB.
P_0–P_7	32–39	32–39	5–12	**PIXEL SELECT INPUTS (TTL COMPATIBLE).** See pixel and overlay data interface section for details P_0 is the LSB. Unused inputs should be connected to GND.
$\overline{RD}$	6	6	15	**READ CONTROL INPUT (TTL COMPATIBLE).** To read data from the device, $\overline{RD}$ must be a logical zero. RS_0–RS_2 are latched on the falling edge of $\overline{RD}$ during microprocessor read operations.
RS_0–RS_2	17–19	17, 18	26,27†	**REGISTER SELECT INPUTS (TTL COMPATIBLE).** RS_0–RS_2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 8.
$\overline{SENSE}$	1	1		**SENSE OUTPUT (TTL COMPATIBLE).** $\overline{SENSE}$ is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that $\overline{SENSE}$ may not be stable while $\overline{SYNC}$ is toggling.
SETUP	23			**SETUP CONTROL INPUT.** Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.

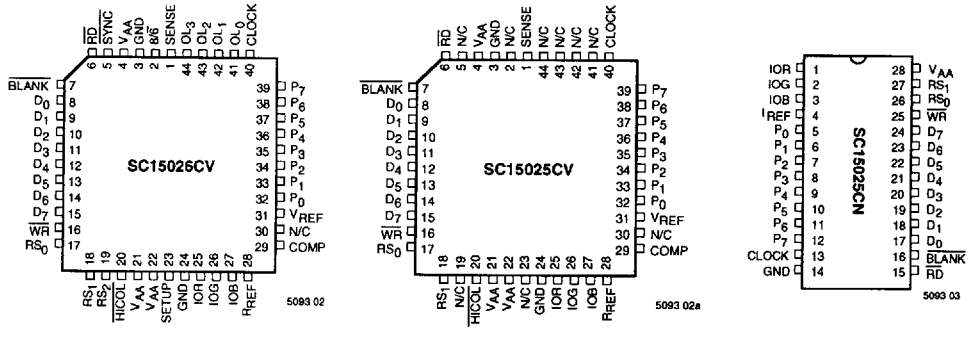
3

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER SC15026 PLCC	PIN NUMBER SC15025 PLCC	PIN NUMBER SC15025 DIP	DESCRIPTION
$\overline{SYNC}$	5			**COMPOSITE SYNC CONTROL INPUT (TTL COMPATIBLE).** A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). $\overline{SYNC}$ does not override any other control or data input, as shown in Fig. 3 and 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
V_{AA}	4, 21, 22	4, 21, 22	28	**ANALOG POWER.** All V_{AA} pins must be connected.
V_{REF}	31	31		**VOLTAGE REFERENCE INPUT.** If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an internal voltage reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to V_{AA}, as shown in Figures 5 and 6. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum. When using internal reference this pin should not drive any external circuitry except for the decoupling capacitor.
$\overline{WR}$	16	16	25	**WRITE CONTROL INPUT (TTL COMPATIBLE).** RS_0–RS_2 are latched on the falling edge of $\overline{WR}$, and D_0–D_7 data is latched on the rising edge of $\overline{WR}$ during microprocessor write operations.

NOTE: †RS_2 is not available on the SC15025. *$8/\overline{6}$ is only available on the SC15026.

CONNECTION DIAGRAMS



NOTE: N/C pins may be left unconnected without affecting the performance of the SC15025/SC15026.

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

The SC15025/SC15026 supports a standard microprocessor bus interface allowing direct access to the address register, command register, color look up table, overlay registers, pixel mask register, extended index register, and extended data register.

The RS_0-RS_2 register select inputs, in conjunction with the state of the Internal Programming Flag (IPF) and the Extended Register Programming Flag (ERPF) (bit D_4 of the command register), specify the microprocessor access mode as described in Table 1. The 8-bit address register is used to access both the color look-up table and the overlay registers. Note that the IPF flag is not directly accessible by the microprocessor. The IPF flag can only be set by a special sequence described in the Command Register section.

Reading and Writing Color Lookup Table and Overlay Color Data

In order to read color data, the RS_0-RS_2 inputs must be set to RAM read mode or overlay read mode. The microprocessor reads color data by loading the address of the color look up table or the overlay location being read into the address register. The color information is then copied from the location specified by the address register to the RGB

register and the address register is incremented to the next location. After the microprocessor completes three successive reads (of 6 or 8 bits of each red, green and blue), the contents of the lookup table or overlay location specified by the address register is copied into the RGB register and the address register is incremented again. This feature allows a block of color data to be read by writing to the starting address and performing continuous read cycles until the entire block has been read.

In order to write color data, the RS_0-RS_2 inputs must be set to RAM write mode or overlay write mode. The microprocessor writes color data by writing the address of the color lookup table or the overlay location being modified into the address register. After the microprocessor completes three successive writes (of 6 or 8 bits of each red, green and blue), the three bytes of color information are concatenated and written to the location specified by the address register. Once the location has been written, the address register is incremented to the next location to prepare for another write sequence. This feature allows a block of color data to be written by writing to the starting address and performing continuous write cycles until the entire block has been written.

When accessing the color lookup table, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay registers, the address register increments following a blue read or write cycle. However, while accessing the overlay registers, the four most significant bits of the address register (ADDR4–7) are ignored, as shown inTable 8.

The microprocessor interface access is asynchronous to the pixel clock. Data transfers between the color lookup table/overlay registers and the RGB registers occur in the period between microprocessor accesses and are synchronized by internal logic.

The address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 8, to keep track of the red, green and blue read/write cycles. During microprocessor writes these bits are reset to zero and are not reset when the microprocessor reads the address register. The microprocessor only has access to the first eight bits (ADDR0-7) of the address register which are used to address the color lookup table locations and overlay registers as shown in Table 8. ADDR0 is the least significant bit when the microprocessor is accessing the color lookup table or overlay registers. The microprocessor can read the address register at any time without altering its contents or changing the current read/write mode.

Data Bus Interface

The 8/$\overline{6}$ input pin, in conjunction with Bit 0 of the Auxiliary Control Register controls whether the microprocessor is reading and writing 8-bits (logic one) or 6-bits (logic zero) of color data each cycle.

During 6 bit operation, the lower six bits of the data bus are used to transfer color data. D_0 is the LSB and D_5 is the MSB. When reading color data, D_6 and D_7 will be logic zero. D_6 and D_7 are ignored during write cycles.

During 8 bit operation D_0 is the LSB and D_7 is the MSB. The full scale current output is about 1.5% lower in 6 bit mode than in 8 bit.

Pixel and Overlay Data Interface

The pixel and overlay data interface logic consists of an 8-bit wide pixel data input port, a 4-bit wide overlay input port, an Input Pixel Clock (CLOCK), and the $\overline{SYNC}$ and $\overline{BLANK}$ signals.

The input pixel bus is usually connected to the pixel output port of a VGA controller. The input pixel and overlay data is latched on the rising edge of the pixel clock except in Pixel Repack Modes 1a and 3a (refer to Pixel Repack Logic section for details). The latched pixel data is sent to the Pixel Repack Logic and converted to internal pixel data.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintian synchronization with the color data, add appropriately weighed currents to the analog outputs, producing the specific output levels required for

Command Register EPRF Bit	IPF	Register Select Input RS_2	RS_1	RS_0	Access Type	Addressed by MPU
0	X	0	0	0	Read/Write	Palette RAM write address register
0	X	0	1	1	Read/Write	Palette RAM read address register
0	X	0	0	1	Read/Write	Palette RAM
0	0	0	1	0	Read/Write	Pixel mask register
0	1	0	1	0	Read/Write	Command register
0	X	1	0	0	Read/Write	Overlay RAM write address register
0	X	1	1	1	Read/Write	Overlay RAM read address register
0	X	1	0	1	Read/Write	Overlay RAM
0	X	1	1	0	Read/Write	Command Register
1	X	0	1	1	Write Only	Extended index register
1	X	0	0	1	Read Only	Extended index register
1	X	0	0	0	Read/Write	Extended data registers
1	X	0	1	0	Read/Write	Command register
1	X	1	X	X	Read/Write	Reserved

Table 1. MPU Addressing Truth Table

(a) Repack Mode 0 Format (8 bit x 1 to 8 bit x 1 mode)

Input Pixel Data	No.: n Bit: P7–0
Internal Pixel Data	No.: n Bit: V7–0

(b) Repack Mode 1 Format (8 bit x 2 to 16 bit x 1 mode)

Input Pixel Data	No.: 2n + 1 Bit: P7–0	2n P7–0
Internal Pixel Data	No.: n Bit: V15–8	n V7–0

(c) Repack Mode 2 Format (8 bit x 3 to 24 bit x 1 mode)

Input Pixel Data	No.: 3n + 2 Bit: P7–0	3n + 1 P7–0	3n P7–0
Internal Pixel Data	No.: Internal Pixel Data n Bit: V23–18	V15–8	V7–0

(d) Repack Mode 3 Format (8 bit x 4 to 24 bit x 1 mode)

Input Pixel Data	No.: 4n + 3 Bit: P7–0	4n + 2 P7–0	4n + 1 P7–0	4n P7–0
Internal Pixel Data	No.: Internal Pixel Data n Bit: discard	V23–18	V15–8	V7–0

5093 04

Figure 2. Pixel Repack Mode Format

video applications, as illustrated in Figures 3 and 4, which detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

Setup

The SETUP input specifies whether a 0 IRE (SETUP = GND) or a 7.5 IRE (SETUP = V_{AA}) blanking pedestal is used. The SC15025 only generates a 0 IRE blanking pedestal, as shown in Figure 4.

The analog outputs of the palette are capable of directly driving a 37.5 ohm load such as a doubly-terminated 75 ohm coaxial cable.

Pixel Repack Logic

The Pixel Repack Logic converts one, two or three bytes of input pixel data into either 8-bit, 16-bit or 24-bit internal pixel data. The pixel repack logic has 6 different operating modes which are defined by bits D_7–D_5 of the command register and the Pixel Repack Register, as shown in Table 2.

Repack Mode 0

In this mode, 8-bit input pixel data and 4-bit overlay data are latched on every pixel clock cycle. The input pixel data (P_7–P_0) is directly converted into 8-bit internal pixel data (V_7–V_0). The internal pixel data has the same clock frequency as the input pixel data. The repack format is shown in Figure 2a.

Repack Mode 1a

In this mode, two bytes of input pixel data (P_7–P_0) are latched and then converted into a 16-bit internal pixel data (V_{15}–V_0). In this mode two bytes of the input pixel data are latched on the rising edge and the falling edge of the pixel clock, respectively. The byte latched on the rising edge is converted into the least significant byte (V_7–V_0) of the internal pixel data. The byte latched on the falling edge is converted into the most significant byte (V_{15}–V_8) of the internal pixel data. The clock frequency of the internal pixel data is the same as the clock frequency of the input pixel data.

Repack Mode 1b

In Repack Mode 1b, two bytes of input pixel data (P_7–P_0) are latched and then converted into a 16-bit internal pixel data (V_{15}–V_0). In this mode, two bytes of the input pixel data are latched on two rising edges of the pixel clock. The low-to-high transition of the $\overline{BLANK}$ signal is used to synchronize the formation of the least significant byte (V_7–V_0) and the most significant byte (V_{15}–V_8). The byte latched by the first rising edge of the pixel clock after $\overline{BLANK}$ goes high is converted into the least significant byte. The byte latched by the second rising edge of the pixel clock after $\overline{BLANK}$ goes high is converted into the most sig-

Pixel Repack Register D_7–D_0								Command Register D_7	D_6	D_5	Repack Mode Number	Repack Mode Name	Input Pixel Data	Internal Pixel Data	Comment
0	0	0	0	0	0	0	0	0	0	0	0	8-bit x 1 to 8-bit x 1 mode	P_7–P_0	V_7–V_0	
0	0	0	0	0	0	0	0	1	x	0	1a	8-bit x 2 to 16-bit x 1 mode	P_7–P_0	V_{15}–V_0	See Note 1
0	0	0	0	0	0	0	0	1	x	1	1b	8-bit x 2 to 16-bit x 1 mode	P_7–P_0	V_{15}–V_0	See Note 1
0	0	0	0	0	0	0	0	0	1	1	2	8-bit x 3 to 24-bit x 1 mode	P_7–P_0	V_{23}–V_0	
0	0	0	0	0	0	0	1	0	1	0	3a	8-bit x 4 to 24-bit x 1 mode	P_7–P_0	V_{23}–V_0	See Note 1
0	0	0	0	0	0	0	1	0	1	1	3b	8-bit x 4 to 24-bit x 1 mode	P_7–P_0	V_{23}–V_0	See Note 1

NOTE 1: In modes 1a and 3a, data is latched on both the rising edge and the falling edge of the pixel clock. In modes1b and 3b, data is latched only on the rising edge of the pixel clock.

NOTE 2: All bits of the pixel repack register are initialized to zero at power-on reset.

Table 2. Definition of the Pixel Repack Logic

nificant byte. The byte latched by the third rising edge of the pixel clock after $\overline{BLANK}$ goes high is converted into the least significant byte of the next internal pixel data. The byte latched by the fourth rising edge of the pixel clock after $\overline{BLANK}$ goes high is converted into the most significant byte of the next internal pixel data. Subsequent bytes are latched in the same manner. The clock frequency of the internal pixel data is half of the clock frequency of the input pixel data. The Repack Mode 1b format is shown in Figure 2(b).

Repack Mode 2

In Repack Mode 2, three bytes of input pixel data P_7–P_0 are latched on three rising edges of the pixel clock and then converted into a 24-bit internal pixel data V_{23}–V_0 as shown in Figure 2(c). The low-to-high transition of the $\overline{BLANK}$ signal is used to form a 24-bit internal pixel data. The byte latched by the first rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the least significant byte (V_7–V_0). The byte latched by the second rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the middle byte (V_{15}–V_8). The byte latched by the third rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the most significant byte. The clock frequency of the internal pixel data is one third of the clock frequency of the input pixel data.

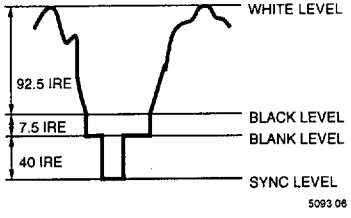
Repack Mode 3a

In Repack Mode 3a four bytes of the input pixel data P_7–P_0 are latched, three bytes are converted into a 24-bit internal pixel data V_{23}–V_0, and the forth byte is discarded, as shown in Figure 2(d). The low-to-high transition of the $\overline{BLANK}$ signal is used to form a 24- bit internal pixel data. The byte latched by the first rising edge of the pixel clock after the $\overline{BLANK}$ goes high is converted into the least significant byte. The byte latched by the falling edge of the same pixel clock is converted into the middle byte. The byte latched by the second rising edge of the pixel clock after the $\overline{BLANK}$ goes high is converted into the most significant byte. The byte latched by the falling edge of this pixel clock is discarded. Subsequent bytes are latched in the same manner. The clock frequency of the internal pixel data in this mode is half of the clock frequency of the input pixel data.

Repack Mode 3b

In Repack Mode 3b four bytes of the input pixel data are latched on the four rising edges of the pixel clock. The low-to-high transition of the $\overline{BLANK}$ signal is used to form a 24-bit internal pixel data. The byte latched by the first rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the least significant byte. The byte latched by the second rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the middle byte. The byte latched by the third rising edge of pixel clock after the $\overline{BLANK}$ goes high is converted into the most significant byte. The byte latched by the fourth rising edge of pixel clock after the $\overline{BLANK}$ goes high is discarded. The clock frequency of the internal pixel data in this mode is one fourth of the clock frequency of the input pixel data.

SC15026 w/o SYNC		SC15026 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



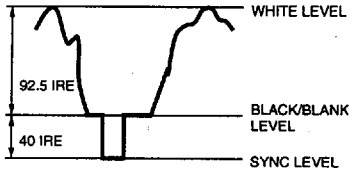
NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Description	SC15026 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω.

Figure 3. Composite Video Output Waveform and Truth Table (SETUP = V_{AA})

SC15025/SC15026 w/o Sync		SC15026 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



NOTE: 75 Ω doubly-terminated load, SETUP = GND, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Description	SC15025 I_{OUT} (mA)	SC15026 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA–SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = GND, V_{REF} = 1.235 V, RSET = 147 Ω.

Figure 4. Composite Video Output Waveform and Truth Table(SETUP = GND)

Color Mode Control Logic

The color mode control logic translates (maps) internal pixel data V_{23}–V_0 into a color index consisting of three components: R_7–R_0 (red), G_7–G_0 (green) and B_7–B_0 (blue). The color index provides an address to the color LUT whose outputs are used to drive the triple DAC. In certain modes the color index can bypass the LUT to directly drive the triple DACs. The Color Mode Control Logic supports six color modes (refer to Table 3 for details).

Color Mode 0

Color Mode 0 is an 8-bit 256 color (pseudo color) mode. Eight bits (V_7–V_0) of the internal pixel data are mapped into the color index as shown in Table 4. P_i is mapped simultaneously to R_i, G_i and B_i (i = 0–7). The LUT in this mode is organized as a 256 x 24 RAM. The output of the color palette RAM (any one of the 256 color entries of the color palette RAM selected by the pixel data) becomes an input to the triple DAC. The lookup table cannot be bypassed in this mode. The overlay RAM can also be used in this mode to give 15 additional colors.

Color Mode 1

Color Mode 1 is the HiCOLOR-15™ (5-5-5) mode. If the D_3 bit of the command register is 1 (as shown in Table 4), V_{14}–V_{10}, V_9–V_5, and V_4–V_0 of the internal pixel data are mapped into R_5–R_1, G_5–G_1 and B_5–B_1, respectively. R_6, G_6 and B_6 are all mapped from D_1 of the command register. R_7, G_7 and B_7 are all mapped from D_2 of the command register. R_0, G_0 and B_0 are zero. In this mode the LUT RAM is organized as four 32 x 8 x 3 color RAMs. The D_1 and D_2 bits of the command register specify which one of the four color LUTs is used. The V_{14}–V_{10}, V_9–V_5, and V_4–V_0 will select one of the 32 red, green, and blue entries of the specified LUT to be sent to the red, green, and blue DACs, respectively.

If the D_3 bit of the command register is 0, the color LUT is bypassed (as shown in Table 4). In this case,

Command Register D_7	D_6	D_0	Color Mode Number	Color Mode Name
0	0	0	0	8-Bit pseudo color Mode
1	0	0	1	HiCOLOR-15™ 5-5-5 Mode
1	0	1	2	Extended HiCOLOR-15™ 5-5-5 Mode
1	1	0	3	HiCOLOR-16™ 5-6-5 Mode
0	1	0	4	HiCOLOR-24™ 8-8-8 RGB mode
0	1	1	5	HiCOLOR-24™ 8-8-8 BGR mode
0	0	1		Reserved
1	1	1		

Table 3. Definition of the Color Mode Control Logic

Color Index	Color Mode	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	Comment
Internal Pixel Data	0	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	
	1 (if D_3=1)	D_2	D_1	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	0	D_2	D_1	V_9	V_8	V_7	V_6	V_5	0	D_2	D_1	V_4	V_3	V_2	V_1	V_0	0	
	1 (if D_3=0)	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	0	0	0	V_9	V_8	V_7	V_6	V_5	0	0	0	V_4	V_3	V_2	V_1	V_0	0	0	0	LUT Bypass
	2 (if D_3=1)	D_2	D_1	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	V_{15}	D_2	D_1	V_9	V_8	V_7	V_6	V_5	V_{15}	D_2	D_1	V_4	V_3	V_2	V_1	V_0	V_{15}	
	2 (if D_3=0)	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	V_{15}	0	0	V_9	V_8	V_7	V_6	V_5	V_{15}	0	0	V_4	V_3	V_2	V_1	V_0	V_{15}	0	0	LUT Bypass
	3 (if D_3=1)	D_2	D_1	V_{15}	V_{14}	V_{13}	V_{12}	V_{11}	0	D_2	D_1	V_{10}	V_9	V_8	V_7	V_6	V_5	D_2	D_1	V_4	V_3	V_2	V_1	V_0	0	
	3 (if D_3=0)	V_{15}	V_{14}	V_{13}	V_{12}	V_{11}	0	0	0	V_{10}	V_9	V_8	V_7	V_6	V_5	0	0	V_4	V_3	V_2	V_1	V_0	0	0	0	LUT Bypass
	4	V_{23}	V_{22}	V_{21}	V_{20}	V_{19}	V_{18}	V_{17}	V_{16}	V_{15}	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	V_9	V_8	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	
	5	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	V_{15}	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	V_9	V_8	V_{23}	V_{22}	V_{21}	V_{20}	V_{19}	V_{18}	V_{17}	V_{16}	

NOTE 1: D1, D2 and D3 are the second, third, and fourth least significant bits of the command register.

Table 4. Color Modes Truth Table

V_{14}–V_{10}, V_9–V_5, and V_4–V_0 of the internal pixel data are mapped into R_7–R_3, G_7–G_3 and B_7–B_3, respectively. All other bits of the color index are zero. The V_{14}–V_{10}, V_9–V_5, and V_4–V_0 directly drive the five most significant bits of the red, green, and blue DACs, respectively. Overlay RAM is ignored in this mode.

Color Mode 2

Color mode 2 is the extended HiCOLOR-15™ (5-5-5) mode. If the D_3 bit of the command register is 1, the lookup table is not bypassed (Table 4) and the internal pixel data V_{14}–V_{10}, V_9–V_5, and V_4–V_0 is mapped into the R_5–R_1, G_5–G_1 and B_5–B_1, respectively. V_{15} is mapped into R_0, G_0, and B_0 simultaneously. The R_6, G_6, and B_6 are mapped from the D_1 bit of the command register. The R_7, G_7, and B_7 are mapped from the D_2 bit of the command register. The LUT is organized as an eight 32 x 8 x 3 LUT (4 even LUTs and 4 odd LUTs). Either an even LUT or an odd LUT can be selected by V_{15} *on the fly*. The D_1 and D_2 bits of the command register specify which one of the 4 even and four odd LUTs is used. The V_{14}–V_{10}, V_9–V_5, and V_4–V_0 will select one of the 32 red, green, and blue entries of the specified even or odd LUT to be sent to the red, green, and blue DACs, respectively. In this way, two 32 x 8 x 3 LUTs are available simultaneously and can be selected by V_{15} on the fly.

If the D_3 bit of the command register is 0, the lookup table is bypassed. In this case, V_{14}–V_{10}, V_9–V_5, and V_4–V_0 of the internal pixel data are mapped into R_7–R_3, G_7–G_3 and B_7–B_3, respectively, and V_{15} is mapped into R_2, G_2, and B_2. All other bits of the color index are zero. Internal pixel data V_{14}–V_{10}, V_9–V_5, and V_4–V_0 directly drive the five most significant bits of the red, green, and blue DACs, and V_{15} drives the sixth most signficant bit of the red, green, and blue DACs simultaneously. Overlay RAM is ignored in this mode.

Color Mode 3

Color Mode 3 is the HiCOLOR-16™ (5-6-5) mode. If the D_3 bit of the command register is 1, the look-up table is not bypassed. In this mode V_{15}–V_{11}, V_{10}–V_5, and V_4–V_0 of the internal pixel data are mapped into R_5–R_1, G_5–G_0, and B_5–B_1, respectively. R_6, G_6, and B_6 are all mapped from D_1 of the command register. R_7, G_7, and B_7 are all mapped form the D_2 bit of the command register. R_0 and B_0 are zero. The LUT in this case is organized as four 32x8 + 64x8 + 32x8 color LUTs. The command register bits D_1 and D_2 will specify which of the four LUTs is used. V_{15}–V_{11}, V_{10}–V_5, and V_4–V_0 will select one of the 32 red, 64 green, and 32 blue entries of the specified palette to be sent to the red, green and blue DACs.

If D_3 of the command register is 0, the lookup table is bypassed (as shown in Table 4). In this case, V_{15}–V_{11}, V_{10}–V_5, and V_4–V_0 of the internal pixel data are mapped into R_7–R_3, G_7–G_2, and B_7–B_3, respectively. All other bits of the color index are zero. As a result, V_{15}–V_{11}, V_{10}–V_5, and V_4–V_0 directly drive the five most significant bits of the red, six most significant bits of the green, and five most significant bits of the blue DACs, respectively. Overlay RAM is ignored in this mode.

Color Mode 4

Color mode 4 is the HiCOLOR-24™ (8-8-8) RGB mode. In this mode, V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 of the internal pixel data are mapped into R_7–R_0, G_7–G_0, and B_7–B_0 respectively. The LUT is organized as a three 256 x 8 RAMs. The LUT can be bypassed if the D_3 bit of the command register is 0. In this case, V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 directly drive the red, green, and blue DACs, respectively. If the D_3 bit of the command register is 1, the look-up table is not bypassed. In this case V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 will select one of the 256 red, green, and blue entries of the palette to be sent to the red, green, and blue DACs, respectively.

Color Mode 5

Color mode 5 is the HiCOLOR-24™ (8-8-8) BGR mode. In this mode, V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 of the internal pixel data are mapped into B_7–B_0, G_7–G_0, and R_7–R_0, respectively. The LUT is organized as a three 256 x 8 RAMs. If D_3 bit of the command register is 0, the lookup table is bypassed. In this case, V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 directly drive the blue, green, and red DACs, respectively. If D_3 bit of the command register is 1, the LUT is not bypassed. In this case V_{23}–V_{16}, V_{15}–V_8, and V_7–V_0 select one of the 256 blue, green, and red entries of the LUT and is sent to the blue, green, and red DACs, respectively.

The operating mode of the SC15025/SC15026 is uniquely determined by a combination of a pixel Repack Mode and a color mode. Table 5 shows all operating modes of the SC15025/SC15026.

Pixel Mask

The internal pixel data (V_{23}–V_0) passes through the pixel mask logic before it addresses the LUT or directly drives the triple DAC. The pixel mask logic can force some or all of these pixel bits to zero by ANDing them with pixel mask register and secondary pixel mask register. The pixel mask register is an 8-bit register and the secondary pixel mask reg ister is a 24-bit register. The bit position of the ANDing operation is determined by the color mode and is shown in Table 6.

The Secondary Pixel Mask Register (S_{23}–S_0) is ANDed with V_{23}–V_0, in

Pixel Repack Register D_7–D_0								Command Register D_7	D_6	D_5	D_0	Repack Mode	Color Mode	Operating Mode	Description
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8-bit pseudo color mode
0	0	0	0	0	0	0	0	1	0	0	0	1a	1	1	HiCOLOR-15™ 5-5-5 mode using both clock edges
0	0	0	0	0	0	0	0	1	0	1	0	1b	1	2	HiCOLOR-15™ 5-5-5 mode using only rising edge
0	0	0	0	0	0	0	0	1	0	0	1	1a	2	3	Extended HiCOLOR-15™ 5-5-5 mode using both clock edges
0	0	0	0	0	0	0	0	1	0	1	1	1b	2	4	Extended HiCOLOR-15™ 5-5-5 mode using only rising edge
0	0	0	0	0	0	0	0	1	1	0	0	1a	3	5	HiCOLOR-16™ 5-6-5 mode using both clock edges
0	0	0	0	0	0	0	0	1	1	1	0	1b	3	6	HiCOLOR-16™ 5-6-5 mode using only rising edge
0	0	0	0	0	0	0	0	0	1	1	0	2	4	7	3-byte 8-8-8 RGB mode using only rising edge
0	0	0	0	0	0	0	0	0	1	1	1	2	5	8	3-byte 8-8-8 BGR mode using only rising edge
0	0	0	0	0	0	0	1	0	1	0	0	3a	4	9	4-byte 8-8-8 RGB mode using both clock edges
0	0	0	0	0	0	0	1	0	1	0	1	3a	5	10	4-byte 8-8-8 BGR mode using both clock edges
0	0	0	0	0	0	0	1	0	1	1	0	3b	4	11	4-byte 8-8-8 RGB mode using only rising edge
0	0	0	0	0	0	0	1	0	1	1	1	3b	5	12	4-byte 8-8-8 BGR mode using only rising edge

Table 5. Summary of Pixel Repack Modes and Color Modes

Color Mode \ Internal Pixel Data	V_{23}	V_{22}	V_{21}	V_{20}	V_{19}	V_{18}	V_{17}	V_{16}	V_{15}	V_{14}	V_{13}	V_{12}	V_{11}	V_{10}	V_9	V_8	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0
0																	M_7 S_7	M_6 S_6	M_5 S_5	M_4 S_4	M_3 S_3	M_2 S_2	M_1 S_1	M_0 S_0
1										M_7 S_{14}	M_6 S_{13}	M_5 S_{12}	M_4 S_{11}	M_3 S_{10}	M_7 S_9	M_6 S_8	M_5 S_7	M_4 S_6	M_3 S_5	M_7 S_4	M_6 S_3	M_5 S_2	M_4 S_1	M_3 S_0
2									M_2 S_{15}	M_7 S_{14}	M_6 S_{13}	M_5 S_{12}	M_4 S_{11}	M_3 S_{10}	M_7 S_9	M_6 S_8	M_5 S_7	M_4 S_6	M_3 S_5	M_7 S_4	M_6 S_3	M_5 S_2	M_4 S_1	M_3 S_0
3									M_7 S_{15}	M_6 S_{14}	M_5 S_{13}	M_4 S_{12}	M_3 S_{11}	M_7 S_{10}	M_6 S_9	M_5 S_8	M_4 S_7	M_3 S_6	M_2 S_5	M_7 S_4	M_6 S_3	M_5 S_2	M_4 S_1	M_3 S_0
4, 5	M_7 S_{23}	M_6 S_{22}	M_5 S_{21}	M_4 S_{20}	M_3 S_{19}	M_2 S_{18}	M_1 S_{17}	M_0 S_{16}	M_7 S_{15}	M_6 S_{14}	M_5 S_{13}	M_4 S_{12}	M_3 S_{11}	M_2 S_{10}	M_1 S_9	M_0 S_8	M_7 S_7	M_6 S_6	M_5 S_5	M_4 S_4	M_3 S_3	M_2 S_2	M_1 S_1	M_0 S_0

NOTE: M_7–M_0 are the eight bits of the pixel mask register. S_{23}–S_0 are the twenty-four bits of the secondary pixel mask register.

Table 6. Pixel Mask Logic Truth Table

all modes as shown in Table 6. On the other hand, each bit of the Pixel Mask Register (M_7–M_0) is ANDed with one or more bits of the internal pixel data in a different position, depending on the color mode. When the power is turned on, all bits of the Pixel Mask Register and the Secondary Pixel Mask Register are set to one .

$\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±10% tolerance. Note that $\overline{\text{SYNC}}$ should be logical zero for $\overline{\text{SENSE}}$ to be stable.

Command Register

The command register is an 8-bit register. It can be written to or read by the microprocessor interface at any time. At power-on-reset the register is initialized to logic zero. The command register can be accessed by setting the Internal Programming Flag (IPF) to 1 without using the RS_2 pin (refer to Table 1 for details).

The IPF can be set to one by four consecutive microprocessor reads from the address $RS_0 = RS_2 = 0$, $RS_1 = 1$.

Once the IPF is set to 1, the next microprocessor write to the address $RS_0 = 0$, $RS_1 = 1$, $RS_2 = 0$ will cause the data on the microprocessor bus to be directed to the command register, or the next microprocessor read from the address $RS_0 = 0$, $RS_1 = 1$, $RS_2 = 0$ will read the content of the command register.

The IPF can be reset to zero by any of the following operations:

1. At power on
2. Microprocessor write to any address
3. Microprocessor read from any address other than $RS_0 = 0$, $RS_1 = 1$, $RS_2 = 0$.

The description of the bits in the command register is given in Table 10.

Color Lookup Table (Palette RAM and Overlay RAM)

The color LUT is a high-speed RAM consisting of a 256 x 8 x 3 color palette and a 15 x 24 overlay. The LUT can be accessed by either the color index (R_7–R_0, G_7–G_0 or B_7–B_0) or the MPU interface. The overlay can be accessed by either the four overlay bits (OL_0–OL_3) or the MPU interface.

When the LUT is accessed by the color index and the overlay bits, the address truth table is shown in Table 7. How the MPU interface accesses to the color LUT and the overlay is described in the Microprocessor Interface section.

Extended Index Resister and Extended Data Registers

The SC15025/SC15026 has several extended registers to support advanced features of the device. The RS_0–RS_2 address pins are used by the microprocessor interface to access these registers as shown in Table 1. The ERPF bit (D_4 bit of the command register) determines whether the microprocessor is accessing the standard VGA palette registers or the extended registers. When the ERPF bit is a logic zero, the microprocessor bus is directed to the standard VGA palette registers. When the ERPF bit is a logic one, the microprocessor bus is directed to the Extended Index Register or the Extended Data Registers. The ERPF bit at power-on is reset to zero in order to maintain VGA compatibility.

In order to access the extended registers, the command register is first programmed by the microprocessor. After writing a logic one to the ERPF bit in the command register, the microprocessor bus is directed to the Extended Index Register or the Extended Data Registers. The microprocessor bus will continue to access the extended registers as long as the ERPF bit is a logic one. The ERPF bit must be set to a logic zero in order to access the standard VGA palette registers. Note that when ERPF = 1, the command register can be accessed using the address $RS_0 = 0$, $RS_1 = 1$, $RS_2 = 0$ and IPF does not need to be set to a logic one, as shown in Table 1.

Accessing Extended Data Registers

The Extended Data Registers are indexed registers. These registers can be accessed by first writing the extended index register using the address $RS_0 = RS_1 = 1$, $RS_2 = 0$ and then data can be read from or written to an extended data register using the address $RS_0 = RS_1 = RS_2 = 0$. The extended index register is 8-bits wide and can address 256 locations. Only 9 of the 256 possible locations are used in the SC15025/SC15026 with remaining undefined index values reserved for future use. The 9 extended data registers are listed in Table 9.

OL_3–OL_0	R_7–R_0 G_7–G_0 B_7–B_0	ADDRESSED LOCATION
$0	$00	Palette RAM location 0
$0	$01	Palette RAM location 1
:	:	:
$0	$FF	Palette RAM location 255
$1	$xx	Overlay RAM location 1
$2	$xx	Overlay RAM location 2
:	$xx	:
$F	$xx	Overlay RAM location 15

Table 7. Color Index and Overlay Bits Address Truth Table

	Value	RS_2	RS_1	RS_0	Addressed by MPU
ADDRa, b (counts modulo 3)	00				Red value
	01				Green value
	10				Blue value
ADDR0–7 (counts binary)	$00-$FF	0	0	1	Color Lookup Table
	xxxx 0000	1	0	1	Reserved
	xxxx 0001	1	0	1	Overlay Color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	Overlay Color 15

Table 8. Address Register (ADDR) Operation

Auxiliary Control Register (Index: 08hex)

Bit7–Bit1	Not Used, must be set to zero for compatibility. These bits are reserved for future use.
Bit0	This bit is ORed with 8/6* pin input.
Bit0="0"	Microprocessor reads/writes 6–bit of color data each cycle if 8/6* pin is "0".
Bit0="1"	Microprocessor reads/writes 8–bit of color data each cycle
	At power on reset, Bit0 is set to logic zero.

ID Registers (Index: 09hex–0Chex)

These are 8–bit read only registers which are used to store the identification code of the SC15025/SC15026. The contents of these locations are as follows and cannot be modified by the microprocessor:

Byte #1 (Index 09hex): 01010011 (ASCII code of 'S')
Byte #2 (Index 0Ahex): 00111010 ⟩ Unique for the SC15025/26
Byte #3 (Index 0Bhex): 10110001 ⟩ Unique for the SC15025/26
Byte #4 (Index 0Chex): for version number, the current number is 01000001 (ASCII code of 'A')

Secondary Pixel Mask Register, Low Byte (Index: 0Dhex)

This 8–bit register provides the low byte (S_7–S_0) of the Secondary Pixel Mask Register. The register is ANDed with the input pixel data bits V_7–V_0. The D_7 corresponds to S_7 and D_0 corresponds to S_0. Refer to Table 6 for details. At power–on reset, the register is set to logic one.

Secondary Pixel Mask Register, Middle Byte (Index: 0Ehex)

This 8–bit register provides the middle byte (S_{15}–S_8) of the Secondary Pixel Mask Register. The register is ANDed with the input pixel data bits V_{15}–V_8. The D_7 corresponds to S_{15} and D_0 corresponds to S_8. Refer to Table 6 for details. At power–on reset, the register is set to logic one.

Secondary Pixel Mask Register, High Byte (Index: 0Fhex)

This 8–bit register provides the high byte (S_{23}–S_{16}) of the Secondary Pixel Mask Register. The register is ANDed with the input pixel data bits V_{23}–V_{16}. The D_7 corresponds to S_{23} and D_0 corresponds to S_{16}. Refer to Table 6 for details. At power–on reset, the register is set to logic one.

Pixel Repack Register (Index: 10hex)

This 8–bit register, in conjunction with the D_7–D_5 bits of the command register, sets the pixel repack mode of the device. Refer to Table 2 for details. All bits of this register are initialized to zero at power–on reset.

Table 9. Extended Data Registers

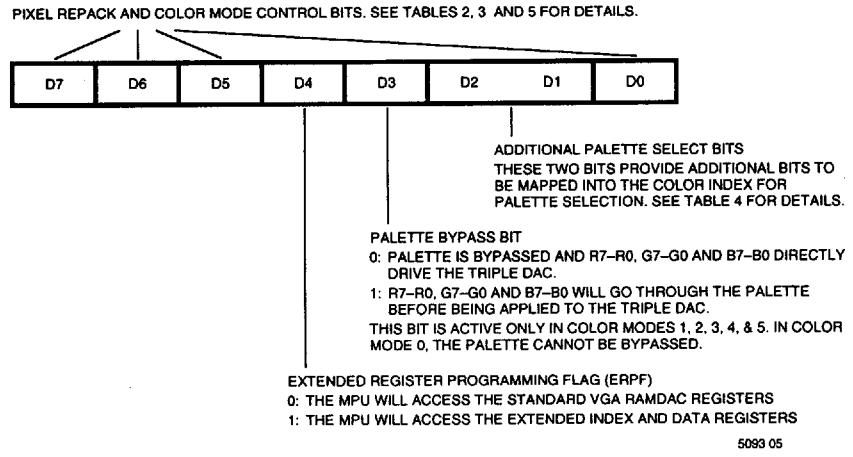


Table 10. Definition of the Command Register

PC BOARD LAYOUT CONSIDERATIONS

The layout should minimize the noise on the power and ground lines by providing good decoupling and shielding all digital inputs. In order to minimize inductive ringing the lead lengths between groups of V_{AA} and GND pins should be minimized.

Separate power and ground planes are recommended to minimize power supply noise. The ground plane should encompass all ground pins, analog output traces, power supply bypass circuitry, and all digital signal traces leading up to the True Color palette.

The True Color palette and any associated analog circuitry should have its own analog power plane. The analog power plane should be isolated from the PCBs digital power plane by a ferrite bead connected at a single point as shown in Figures 5 and 6. The bead should be located within three inches of the True Color palette.

The PCBs digital power plane should provide power to all digital logic on the board.

Ensuring that the PCB digital power and ground planes do not overlay portions of the analog power plane can reduce plane to plane noise coupling.

Supply Decoupling

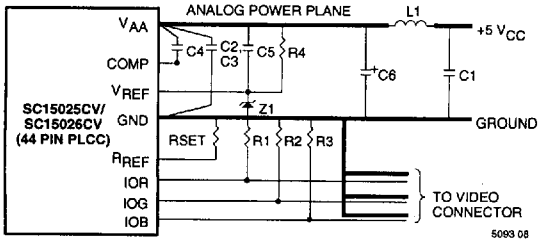
All CMOS and TTL devices on the PCB should be capacitively bypassed. Bypass capacitors should be installed with the shortest possible lead lengths to reduce lead inductance. Each of the two groups of V_{AA} pins should be decoupled to GND using a 0.1 uF ceramic capacitor placed as close as possible to the device. If a high frequency switching power supply is used a three terminal voltage regulator should be used to supply power to the analog power plane.

Digital Signal Interconnect

The digital inputs should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog power plane. Due to the high clock rates the clock lines should be minimized to reduce noise pickup. Active digital input termination resistors should be connected to the regular PCB power plane, not the analog power plane.

Analog Signal Interconnect

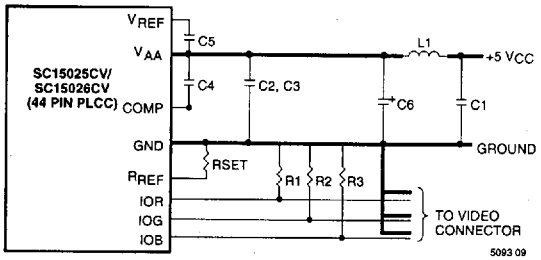
The True Color palette should be located as close as possible to the output connector to minimize noise pickup. The video output signals should overlay the ground plane to maximize the power supply rejection. The analog outputs should each have a 75Ω load resistor connected to ground as close as possible to the True Color palette to minimize reflections.



LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)
Z1	1.2 V Voltage Reference (National Semiconductor LM385BZ-1.2)
R4	1K Ω 5% Resistor

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC15025/SC15026.

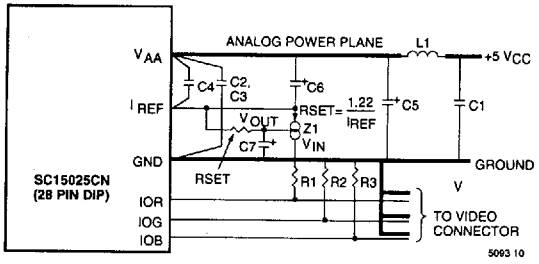
Figure 5. Typical Connection Diagram and Parts List (External Voltage Reference)



LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC15025/SC15026.

Figure 6. Typical Connection Diagram and Parts List (Internal Voltage Reference)



LOCATION	DESCRIPTION
C1–C4	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
C5	47 µF Tantalum Capacitor (Mallory CSR13F476KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
RSET	1% Metal Film Resistor (Dale CMF-55C)

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC15025.

Figure 7. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS

V_{AA} (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to V_{AA} + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Power Supply (V_{AA})	+4.75	5.0	5.25	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (V_{REF})	+1.14	1.235	1.26	V
Current Reference (I_{REF}) (SC15025 only)				
Standard RS-343A	–3	–7.88	–10	mA
PS/2 Compatible	–3	–8.34	–10	mA

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC15025		8	8	8	Bits
SC15026		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC15026				±1	LSB
SC15025				±1	LSB
Differential Linearity Error	D_L				
SC15026				±1	LSB
SC15025				±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND – 0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF

DC ELECTRICAL CHARACTERISTICS (continued)

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC15026					
SETUP = V_{AA}		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC15025		0	0	0	µA
Blank Level					
SC15026		6.29	7.62	8.96	mA
SC15025		0	5	50	µA
Sync Level SC15026		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–0.5		+1.5	V
Output Impedance	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / $\%\Delta V_{AA}$

NOTE: Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, $8/\overline{6}$ = Logical one. For the SC15026, I_{REF} = –7.88 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Since the SC15026 has 6-bit DACs (in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

ANALOG OUTPUT LEVELS—PS/2 COMPATIBILITY

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC15026					
SETUP = V_{AA}		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
SC15025		0	5	50	µA
Blank Level					
SC15026		6.6	8	9.4	mA
SC15025		0	5	50	µA
Sync Level		0	5	50	µA

NOTE: Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, $8/\overline{6}$ = Logical one. For the SC15025CN, I_{REF} = 8.34 mA.

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	125 MHz Devices			110 MHz Devices			80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock Rate (Repack Mode 0)	F_{MAX}			125			110			80			66	MHz
Clock Rate (Repack Mode 1a, 3a)	F_{MAX}			80			65			50			50	MHz
Clock Rate (Repack Mode 1b, 2, 3b)	F_{MAX}			125			110			80			66	MHz
Clock and Data Feedthrough*			-30			-30			-30			-30		dB
Glitch Impulse*			75			75			75			75		pV–sec
DAC to DAC Crosstalk			-23			-23			-23			-23		dB
Analog Output Skew				2			2			2			2	ns
V_{AA} Supply Current**	I_{AA}		180	220		180	220		180	220		180	220	mA

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** At F_{MAX}. I_{AA} (typ) at V_{AA} = 5.0 V. I_{AA} (max) at V_{AA} = 5.25 V.

TIMING WAVEFORMS

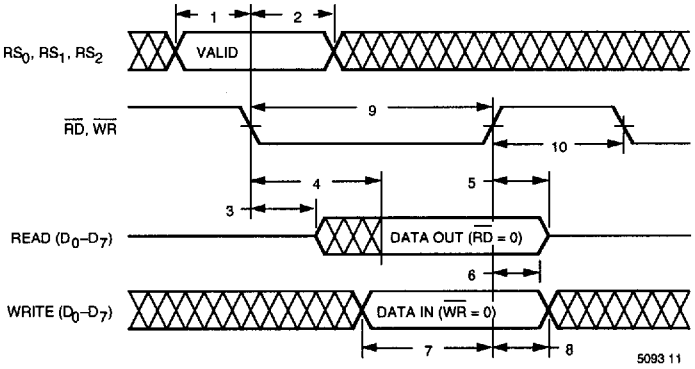


Figure 7. MPU Read/Write Timing

Parameter	Symbol	125 MHz Devices			110 MHz Devices			80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RS_0–RS_2 Setup Time	1	10			10			10			10			ns
RS_0–RS_2 Hold Time	2	10			10			10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20			20			20	ns
Read Data Hold Time	6	5			5			5			5			ns
Write Data Setup	7	10			10			10			10			ns
Write Data Hold Time	8	10			10			10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			4•P13			4•P13			ns

TEST CONDITIONS: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one for the SC15025CV and SC15026CV. For the SC15025CN, I_{REF} = -7.88 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D_0–D_7 output load ≤ 50 pF.

TIMING WAVEFORMS (continued)

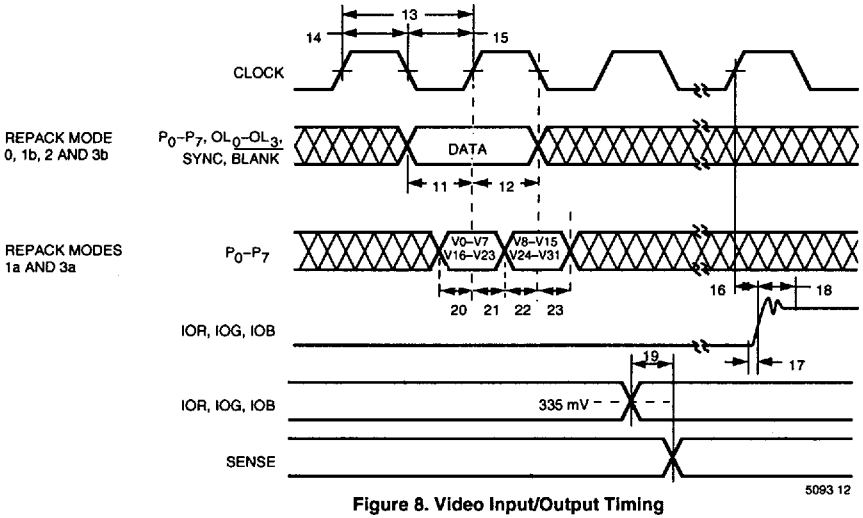


Figure 8. Video Input/Output Timing

NOTE 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
NOTE 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB.
NOTE 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Parameter	Symbol	125 MHz Devices			110 MHz Devices			80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Pixel and Control Setup Time	11	2			2			2			2			ns
Pixel and Control Hold Time (Repack Mode 0 and Repack Mode 2 and Repack Mode 1b and 3b)	12	1			1			2			2			ns
Pixel and Control Setup Time LSB (Repack Mode 1a, 3a)	20	-2.0			-2.0			-2.0			-2.0			ns
Pixel and Control Hold Time LSB (Repack Mode 1a, 3a)	21	6.0			6.0			6.0			6.0			ns
Pixel and Control Setup Time MSB (Repack Mode 1a, 3a)	22	-2.0			-2.0			-2.0			-2.0			ns
Pixel and Control Hold Time MSB (Repack Mode 1a, 3a)	23	6.0			6.0			6.0			6.0			ns
Clock Cycle Time	13	8			9.1			12.5			15.5			ns
Clock Pulse Width High Time	14	3			3.5			4			5			ns
Clock Pulse Width Low Time	15	3			3.5			4			5			ns
Clock Cycle Time (Repack Mode 1a, 3a)	13	12.5			15.4			20			20			ns
Clock Pulse Width High Time (Repack Mode 1a, 3a)	14	4.5			6			8			8			ns
Clock Pulse Width Low Time (Repack Mode 1a, 3a)	15	4.5			6			8			8			ns
Analog Output Delay	16			30			30			30			30	ns
Analog Output Rise/Fall Time	17		2			2.5			3			3		ns
Analog Output Settling Time*	18		8			9			12			15		ns
$\overline{\text{SENSE}}$ Output Delay	19		1			1			1			1		µs

TEST CONDITIONS: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one for the SC15026CV. For the SC15025CN, I_{REF} = -7.88 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D_0–D_7 output load ≤ 50 pF.

TIMING WAVEFORMS (continued)

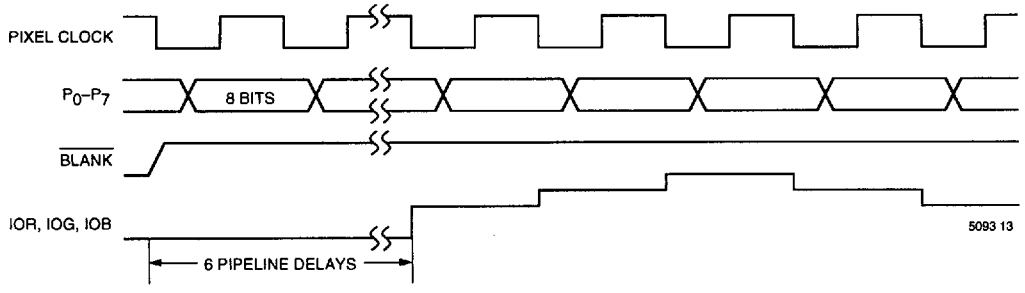


Figure 9. Repack Mode 0 Timing

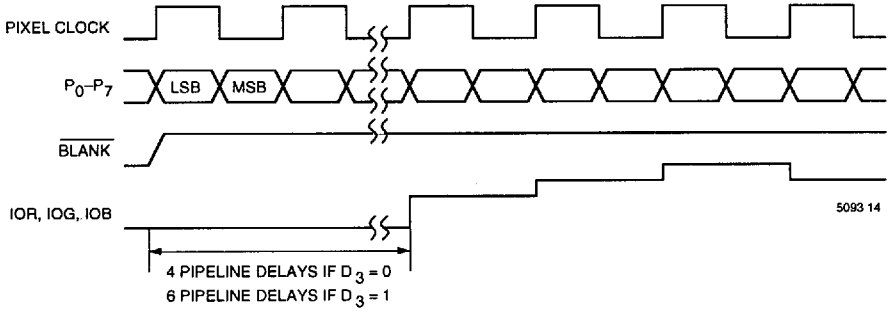


Figure 10. Repack Mode 1a Timing

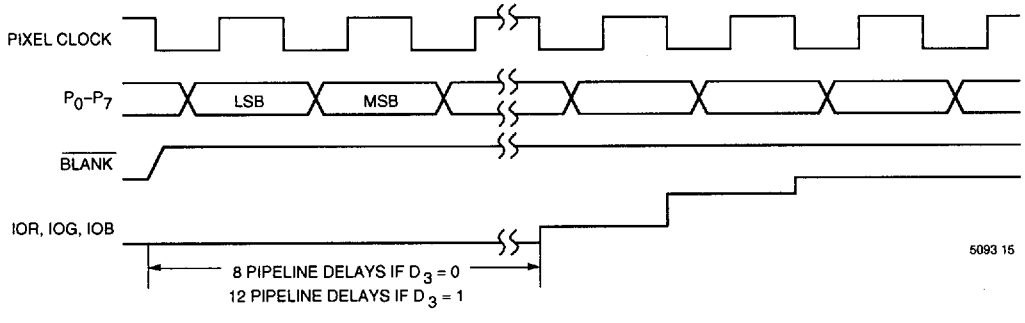


Figure 11. Repack Mode 1b Timing

3

TIMING WAVEFORMS (continued)

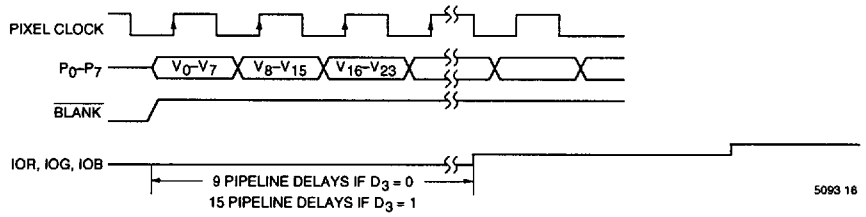


Figure 12. Repack Mode 2 Timing

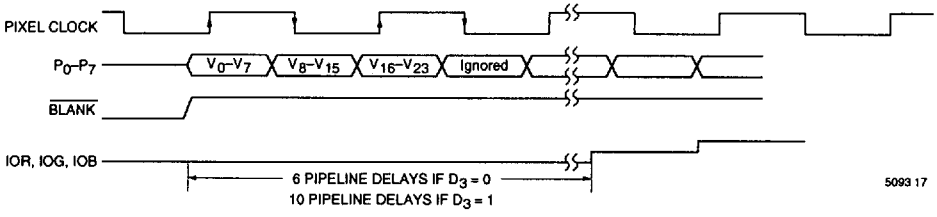


Figure 13. Repack Mode 3a Timing

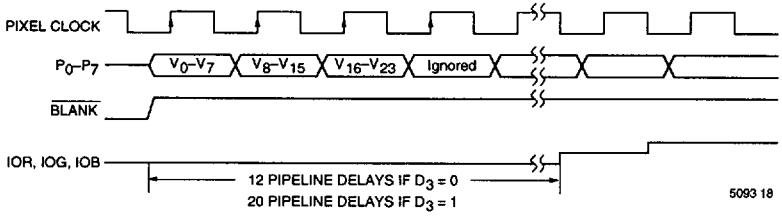


Figure 14. Repack Mode 3b Timing

Parameter	Symbol	125 MHz Devices			110 MHz Devices			80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Pipeline Delay (Repack Modes 0, 1, 2 and 3)		4		20	4		20	4		20	4		24	Clocks

TEST CONDITIONS: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, $8/\overline{6}$ = Logical one for the SC15026CV. For the SC15025CN, I_{REF} = -7.88 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D_0–D_7 output load ≤ 50 pF.

ORDERING INFORMATION

Part No.	Color Lookup Table	Ref. Type	Overlay Registers	Sync. Gen.	Pixel Clock (Max.)			Package	Ambient Temp. Range
					Repack Mode 0	Repack Mode 1a, 3a	Repack Mode 1b, 2, 3b		
SC15026CV-125	256 x 24	V_{REF}	15 x 24	yes	125 MHz	85 MHz	125 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15026CV-110	256 x 24	V_{REF}	15 x 24	yes	110 MHz	65 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15026CV-80	256 x 24	V_{REF}	15 x 24	yes	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15026CV-66	256 x 24	V_{REF}	15 x 24	yes	66 MHz	50 MHz	66 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15025CV-125	256 x 24	V_{REF}	—	no	125 MHz	80 MHz	125 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15025CV-110	256 x 24	V_{REF}	—	no	110MHz	65 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15025CV-80	256 x 24	V_{REF}	—	no	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15025CV-66	256 x 24	V_{REF}	—	no	66 MHz	50 MHz	66 MHz	44-pin Plastic J-Lead	0° to +70°C
SC15025CN-80	256 x 24	I_{REF}	—	no	80 MHz	50 MHz	80 MHz	28-pin 0.6" Plastic DIP	0° to +70°C
SC15025CN-66	256 x 24	I_{REF}	—	no	66 MHz	50 MHz	66 MHz	28-pin 0.6" Plastic DIP	0° to +70°C